Modeling Wilkinson Combiner/Divider at High Microwave Frequencies

A Wilkinson power combiner/divider is a three port microwave circuit frequently used as a building block for more complex circuits like amplifiers, mixers and antenna feeding networks. The simplest variant of the circuit performs equal amplitude and equal phase combining of two input signals. In well designed Wilkinson combiners, the isolation between the input ports at the operating frequency is substantial. A high isolation value is the basic motivation to implement the circuit in various applications. The circuit can be used in the opposite direction, i.e. for dividing an input signal in two equal amplitude and equal phase output signals.

In its simplest form, a circuit has a single section and performs two-way combining/dividing. Due to high demand for versatile combiner/divider components, numerous modifications of the basic circuit topology have been made in the past. These modifications include circuits performing combining/dividing with unequal amplitudes, multi-way signal combining/dividing, bandwidth extension by utilizing multisection topologies etc. Recently, much attention of the research community has been focused on suppression of a parasitic bandwidth occurring at the third harmonic of the operating frequency and operation in dual or multiple, non-harmonically related bands.

However, there are practical situations where even the design of basic, one section, two way combining/dividing structure can be very challenging. The typical example of such a situation is a design of Wilkinson combiner/divider at high microwave frequencies where the effects of discontinuities and component parasitics become significant.

This application note describes a practical aspect of designing a divider/combiner for high frequency of operation using powerful WIPL-D Microwave environment. It provides the step-by-step guide to accurately account for the effects occurring in a real-world circuit, make necessary trade-offs between important circuit performance and achieve first time right design.

Modeling with Analytic Schematic Elements

The schematic of the simplest, one section, two-way Wilkinson microstrip combiner/divider utilizing analytic elements from WIPL-D Microwave microstrip library is presented in Fig. 1. The circuit comprise two quarter wavelength transmission lines connected together directly at one end, and a resistor connected between the other ends of the transmission lines. For the case of equal amplitude combiner/divider in a 50 Ω system, a resistance of the resistor is 100 Ω, and the characteristic impedance of both transmission lines is 50 $\sqrt{2}$ Ω (~70.7 Ω). Due to the symmetry, equal amplitude, in-phase combining/dividing is automatically ensured. A section of 50 Ω transmission line is connected at each of the three ports. These lines are used to make connections with other circuits and do not influence the performance. A substrate chosen for this design has a relative dielectric constant value εr=3.5, and thickness h=0.254 mm. At the operating frequency of 24 GHz quarter wavelength line with characteristic impedance of 70.7 Ω is W=0.29 mm wide and L=1.98 mm long.

Simulated S parameters of Wilkinson combiner/divider presented in Fig. 1 are displayed in Fig. 2. All the ports are well matched with return loss values exceeding 25 dB in the frequency range 22-26 GHz. Isolation at the operating frequency is approximately 32 dB decreasing to approximately 25 dB at the band edges.

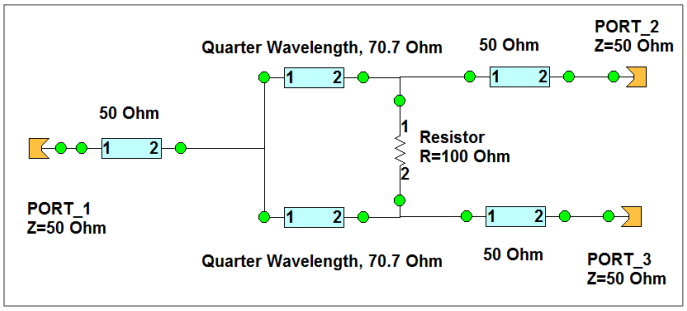

Figure 1. Schematic of the one section, two way microstrip Wilkinson combiner/divider in WIPL-D Microwave.

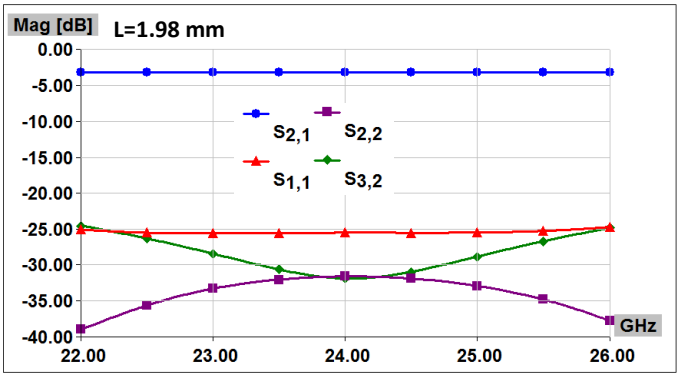

Figure 2. Simulated S parameters of schematic from Fig. 1.

The schematic of the circuit shown in Fig. 1 is idealized, as it doesn't address some important practical aspects a designer encounters when designing a real-world circuit. However, the S parameters presented in Fig. 2 can be regarded as a baseline for further discussion.

The first practical aspect that should be considered is providing conditions for a physical connection of a surface mounted device (SMD) resistor which is a preferred technology for the resistors in modern printed circuits. SMD resistors are available in different sizes which implies different dimensions of the pads required to attach (solder) the resistor in the circuit. For a particular resistor size chosen (0603) the recommended dimensions are WPad=0.5 mm for the width and LPad=0.3 mm

for the length. Another practical aspect arising from the resistor connection is the necessity to divide continuous transmission line section of length L from Fig. 1 in two pieces, Ls and Lc, is, as illustrated in Fig. 3, where a detailed microstrip schematic of combiner/divider is presented. The schematic includes adequate models of all of the discontinuities occurring in the real-world combiner/divider microstrip circuit - an ideal wire connection preceding port 1 of Fig. 1 should be replaced with a T-junction, right angle bends between Ls and Lc sections should be introduced, and dimensionless connections between the resistor and two transmission lines should be modeled with a microstrip T-junction.

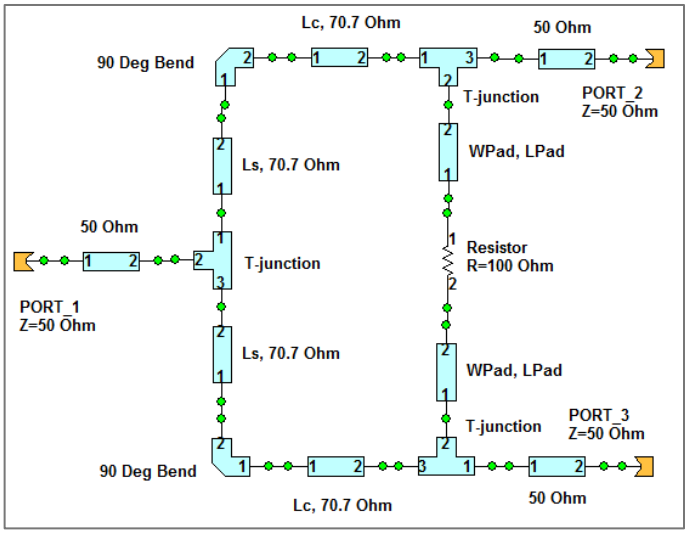

Figure 3. Detailed schematic of microstrip Wilkinson combiner/divider in WIPL-D Microwave including discontinuities and mounting pads of a resistor.

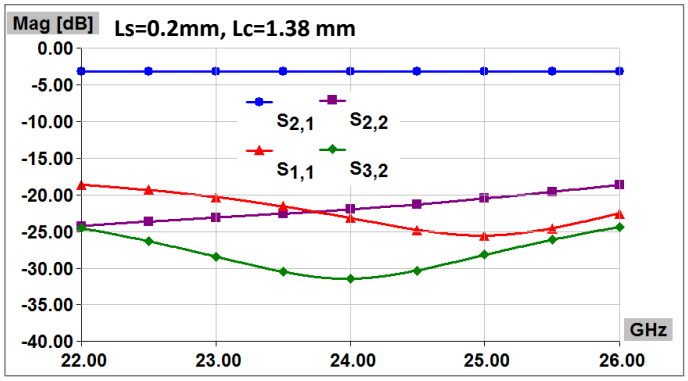

Figure 4. Simulated S parameters of schematic from Fig. 3.

With the introduction of resistor connection details, the performance of the combiner/divider circuit changes. It was necessary to vary the length of the section Lc to recover the maximum isolation value at the operating frequency. The length Ls has been fixed to value of 0.2 mm. Optimum performance has been achieved with Lc=1.38 mm. Results after optimization are presented in Fig. 4. Due to the presence of the resistor pads and the discontinuities, the total length of the transmission lines is smaller than in the previous case. Moreover, the shape of the return loss curves is altered as the minima are shifted away from the operated frequency. However, the overall performance of the combiner/divider can still be regarded as very good as the return losses are better than 20 dB and isolation is better than 25 dB in the whole 22-26 GHz bandwidth.

Modeling with EM Component

It has been illustrated in the previous section that the performance of an ideal combiner/divider can be noticeably changed when more realistic model based on circuit analytical elements is introduced. WIPL-D Microwave design environment provides an additional tool to a designer to further explore the effects of non-idealities - the Wilkinson combiner/divider circuit can be modeled as an EM component. The EM component itself is presented in Fig. 5, while a circuit schematic used for analyzing the combiner/divider circuit is shown in Fig. 6. The results of the simulations are presented in Fig. 7-9.

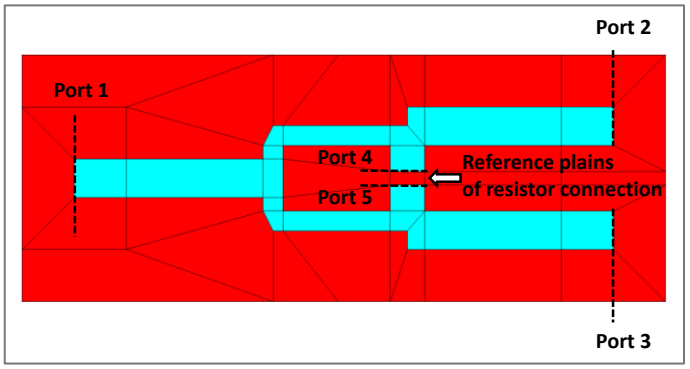

Figure 5. EM component model of Wilkinson combiner/divider from Fig. 3.

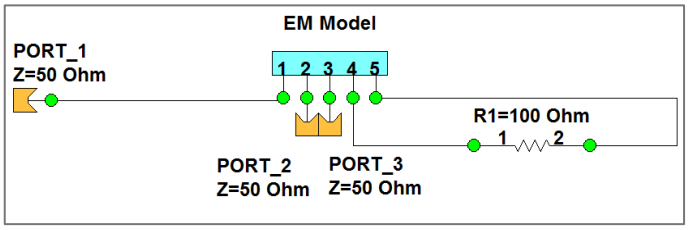

Figure 6. WIPL-D Microwave schematic of Wilkinson combiner/divider using EM component from Fig. 5.

Analyzing S parameters presented in the figures, it becomes apparent that the performance of the combiner/divider as presented in Fig. 4 is not practically achievable. The circuit can be optimized either for one of the return losses, input or output, or for the isolation. The length of Lc section is considerably different for each of the case considered and is indicated in the figures. Additionally, a picture illustrating circuit layout is provided as an inset in each figure. These insets together with Fig. 5 best illustrate the basic reason for the significant influence of resistor connection to combiner/divider performance at high

frequency of operation, which is the high ratio of the resistor pad length and width to the length Lc of a transmission line section. In other words, at high frequencies, resistor connection requires an area with a significant electrical length and width. That is the main reason for drastic change in performance comparing to the case of ideal connections presented in Fig. 1.

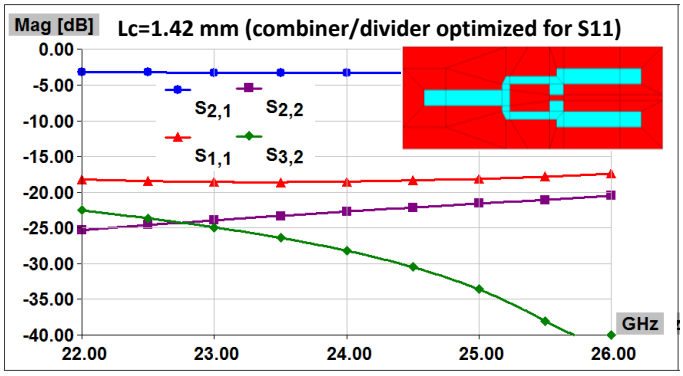

Figure 7. S parameters of schematic from Fig. 6 optimized for S11.

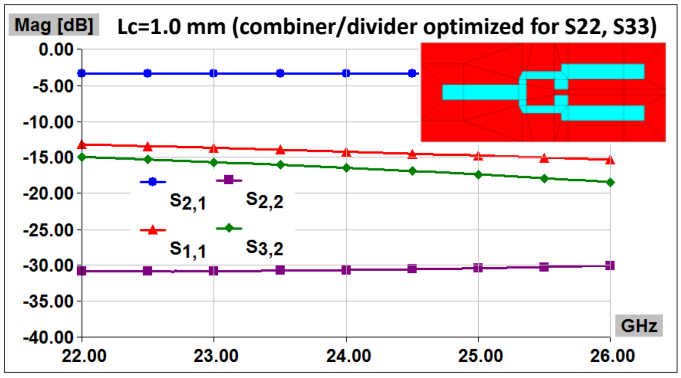

Figure 8. S parameters of schematic from Fig. 6 optimized for S22 and S33.

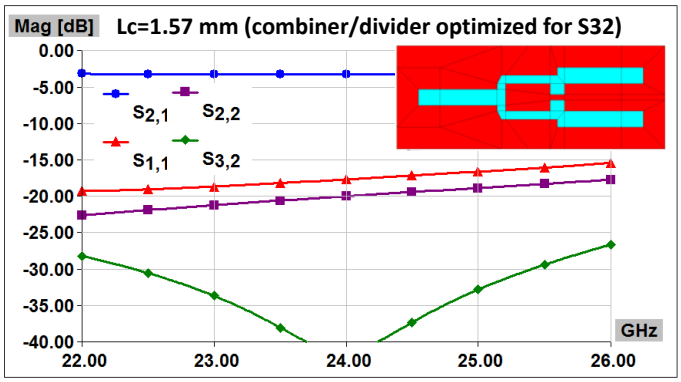

Figure 9. S parameters of schematic from Fig. 6 optimized for S32.

For Lc=1.42 mm input return loss has a minimum value of approximately 18 dB which is almost constant within the frequency band. On the other hand, a value for Lc of 1.0 mm provides almost constant return loss at ports 2 and 3 of approximately 30 dB. Depending on the particular application, one of the two return loss values might be a critical parameter in the design and a designer may opt to accept values of other S parameters and select the circuit design which provides a high return loss value required.

However, as pointed out earlier, the basic motivation to utilize the Wilkinson power combiner/divider is to provide high value for the isolation between ports 2 and 3, or otherwise much simpler Y junction structure can be used. Accordingly, a value of 1.57 mm for Lc, corresponding to the case presented in Fig. 9, is the best choice for most applications. The calculated isolation values are better than 40 dB at the central operating frequency decreasing to approximately 27 dB at the edges of the 22-26 GHz frequency band. It is interesting to notice that these values are higher than the ones found as an optimal for the schematic presented in Fig. 3. Such an outcome again signifies the limited accuracy of analytic models and the importance of electromagnetic analysis. Values of the return losses are approximately 15 dB within the band of interest, which makes the circuit viable for most applications.

Modeling SMD Resistor

In previous discussion SMD resistor has been represented solely as a resistance R. However, the physical construction of a resistor and the attachment to the pads both cause the effects that must be taken into account for accurate modelling. Equivalent circuit of an SMD resistor mounted on a printed circuit board (PCB) is presented in Fig. 10.

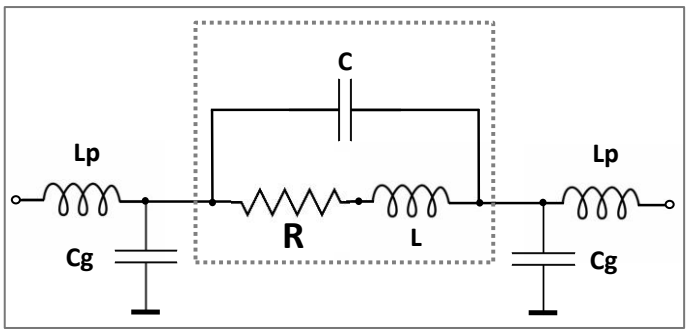

Figure 10. Equivalent circuit of an SMD resistor.

The parasitic effects introduced by resistor internal construction can be modeled with series inductance L and parallel capacitance C. Values of these elements are usually provided by a manufacturer. A connection to the pads adds a series inductance Lp and capacitance to ground Cg. Actual values of these quantities are dependent on εr and h of a substrate used for circuit fabrication, therefore they depend on the particular implementation. To a certain degree, modeling of the pads has already been introduced with EM component model from Fig. 5. However, to completely conform to the physical reality, the location of the reference plains for EM analysis should be aligned with the places of resistor connection, as demonstrated in Fig 11. A complete schematic used to analyze the

combiner/divider circuit, including the modeling of 0603 size 100 Ω SMD resistor, is presented in Fig. 12.

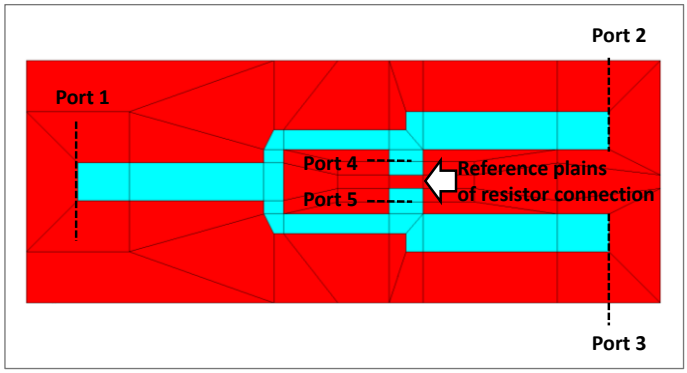

Figure 11. Modified EM component with shifted reference planes of SMD resistor connection.

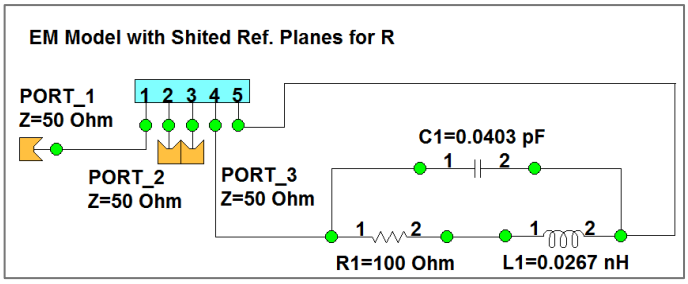

Figure 12. Modified schematic of Wilkinson combiner/divider with a model of 100 Ω resistor.

The results of the simulation of the circuit from Fig. 12 with Lc=1.57 mm, i.e. as previously optimized for isolation, are presented in Fig. 13. It is evident that a very high isolation value of more than 40 dB from Fig. 9 has changed to an average value of approximately 15 dB. The return loss values are slightly changed as well with an average value of approximately 17 dB.

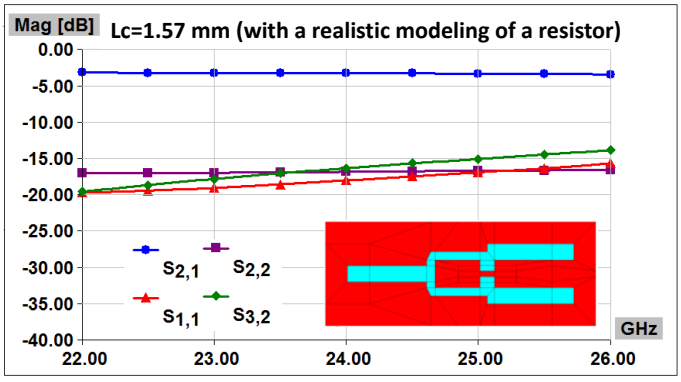

Figure 13. Re-simulated S parameters of Wilkinson combiner/divider optimized for S32 with an ideal resistor.

With the help of additional simulations in WIPL-D Microwave design environment, it has been found that the main reason for reduced isolation is due to the parasitics arising from the internal resistor construction. The contribution of the resistor reference plain alignment, in this particular case, has been found to be marginal having an impact in reducing an isolation value by 0.8 dB.

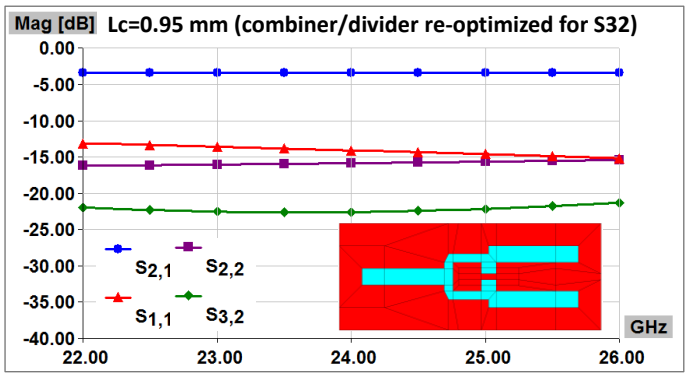

Figure 14. S parameters of Wilkinson combiner/divider re-optimized for S32 including the model of SMD resistor.

To recover a high isolation value, an optimization of the schematic from Fig. 12 has been performed resulting in the optimal performance as presented in Fig. 13. The optimum isolation value of approximately 22 dB has been achieved with Lc=0.95 mm. As a final remark, it should be emphasized that it is of crucial importance to tightly control resistor placement during fabrication, or otherwise the performance of the circuit could easily move away from the one presented in Fig. 14.

Conclusion

The accurate modeling of the effects occuring at high microwave frequencies is the key to successful design of a Wilkinson power combiner/divider. WIPL-D Microwave provides a complete environment required for a design of these circuits including circuit and electromagnetic co-simulation.

Example of a design cycle has been provided. Thecycle starts with the analysis of an ideal, by-the-book circuit schematic, continues to a more detailed schematic with models for microstrip discontinuities, and is then further expanded with the introduction of an EM component to model a complete microstrip circuit with high accuracy. Finally, the impact of a real-world resistor is demonstrated. The impact of each modeling step to degradation of circuit performance comparing to an ideal circuit is illustrated and explained in details. A designer is therefore provided with a clear understanding of what to expect and how to mitigate the potential problems at early stages of the design - it will be a good practice to utilize the smallest resistor size avaialbe, and, if possible, pick a substrate so that line-to-resistor-pad length ratio is maximized.