Linear Transistor Modeling Using Equivalent Circuits

A basic data set typically accompanied discrete, general purpose microwave transistors includes tables of small signal S parameters vs. frequency for several biasing points. S parameters presented in the tables are obtained by measurements on large number of samples. Due to the tolerances in the manufacturing process, there is a spread of characteristics from one transistor to another, and the data listed represent an average result. Therefore, the S parameters provided are the characteristics of so-called average device.

Data supplied for an average device are sufficient to carry out linear amplifier design using a linear circuit simulator. However, as tabulating an extensive set of data covering whole usable range of operation for a device is not preferred by manufacturers, designs are inevitably limited around one to four biasing points where the measurements have been performed. For any biasing point not included in a data sheet, a designer has to exercise his/her own skills to obtain S parameters by carrying out measurements.

In addition to the tables of S parameter values, some manufacturers supply a linear model of a device in the form of a lumped equivalent circuit. As model parameters are usually given for much extensive set of biasing conditions that the S parameter tables, simulation of an equivalent circuit provides the grounds for much versatile utilization of a device, as a number of additional biasing points may be considered for the design. Besides, for the design of some class of circuits, it is beneficial to know values of certain physical quantities (e.g. knowing input and output capacitance values is a starting point when designing distributed amplifiers). As extraction of values of the equivalent circuit elements has already been performed during model built up, the design of such a circuit can be significantly speeded up.

This application note describes how to implement linear (small signal) model of a typical packaged low power transistor in WIPL-D Microwave.

Small Signal Equivalent Circuit Model

At the beginning of a modeling process a suitable equivalent circuit topology should be selected. Selected topology is always a compromise between accuracy and complexity and reflects physical construction of a transistor. Values of the equivalent circuit elements are determined so that values of S parameters calculated through model simulation are in good agreement with measured S parameters. Even for very good models, some amount of discrepancy compared to measurements may still exist. An effort to eliminate a discrepancy by increasing a number of elements should be carried on very carefully as this can sometimes lead to elements that have no physical meaning or reasonable values (e.g. negative capacitances). Furthermore, a practical effect of improving the model must be considered as discrepancy with respect to an average device might be much smaller than the spread of S parameters within a large number of device samples. Therefore, it is usually a goal of a modeling process to achieve acceptable agreement with minimum number of elements.

In the scope of a previous paragraph, a topology for reasonable small signal model given by a manufacturer for a packaged GaAs High Electron Mobility Transistor (HEMT) is presented in Fig. 1. The model consists of 16 elements. The elements used to model the internal structure of the transistor within a semiconductor die are usually called intrinsic elements. The other elements, used to model the influence of a package to the transistor performance, are called extrinsic elements, or simply package parasitics. Intrinsic elements are bias dependent while the extrinsic are not. The list of the intrinsic and extrinsic elements from Fig. 1 is presented in Table 1.

Table 1. Classification of model elements from Fig. 1.

Extrinsic transistor elements	Intrinsic transistor elements
Rg	Gm
Rd	Tau
Rs	Cgs
Cpgs	Rgs
Cpds	Cgd
Cpgd	Cds
Ls	Rds
Lg	
Ld	

Package parasitics include resistances (Rg, Rs, Rd) and inductances (Lg, Ls, Ld) of transistor gate, source and drain leads respectively. A transistor package adds parasitic capacitances between the electrodes (Cpgs, Cpds, Cpgd). Capacitance between gate and source (Cgs) is bias dependent. Large input transistor resistance in parallel to the capacitance Cgs is modeled with 1 MΩ resistor. Voltage across the input resistance is a control voltage for the current generator in the drain. The transconductance of this generator is Gm and the delay of drain current with respect to the control voltage is Tau. Drain current drives a parallel connection of the resistance Rds and capacitance Cds. A parasitic capacitance between gate and drain has a value Cgd.

To systematically examine the influence of a biasing point to transistor characteristics in WIPL-D Microwave, it is convenient to specify values for extrinsic elements in the schematic, and to define values of intrinsic elements as symbols. In such a way a change of biasing point can be easily accommodated by changing values for the symbols, as presented in Fig. 2.

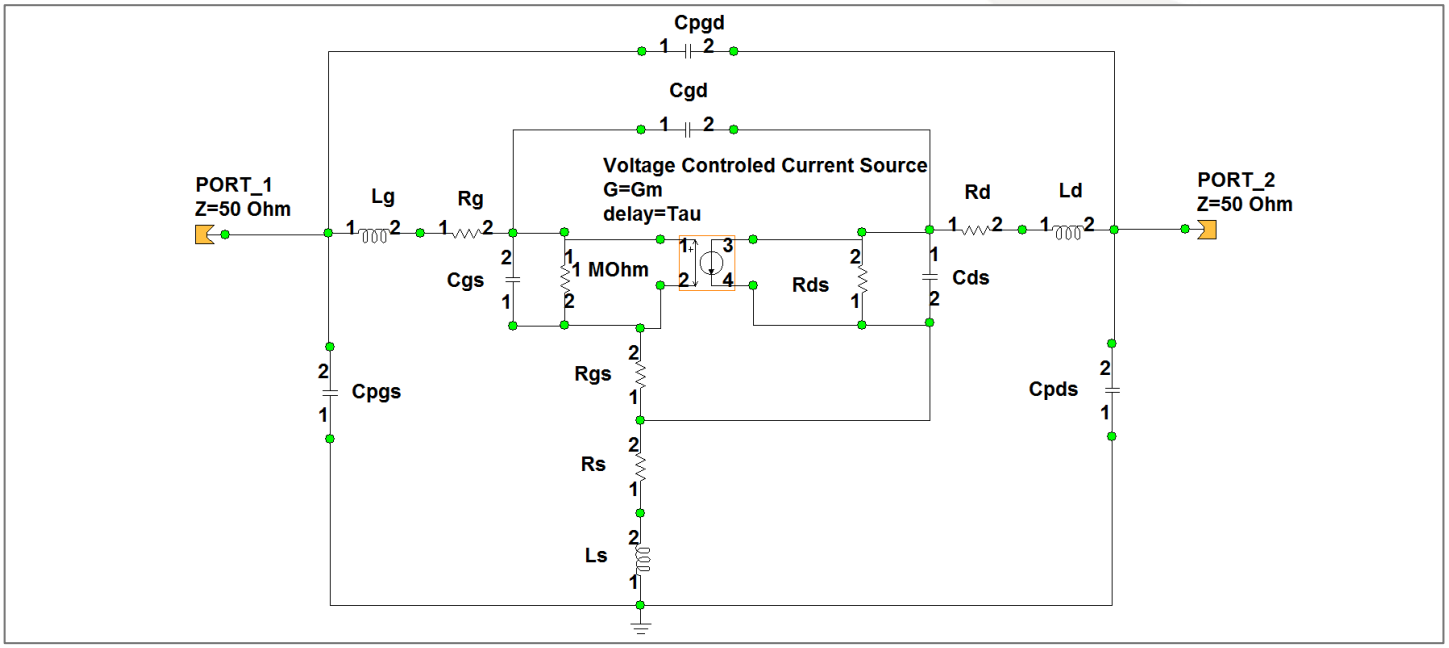

Figure 1. Equivalent circuit model of low power GaAs HEMT transistor implemented in WIPL-D Microwave.

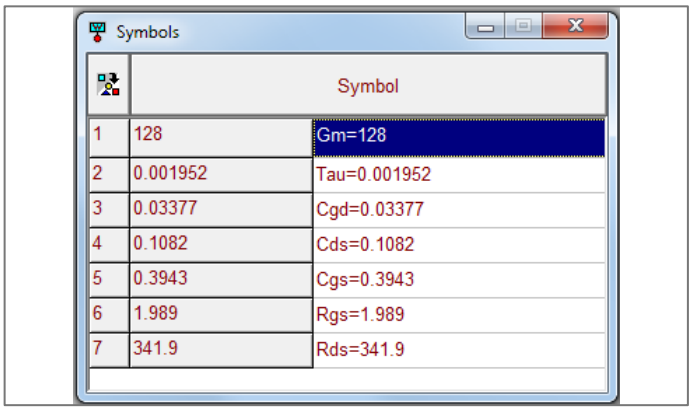

Figure 2. Values of bias dependent equivalent circuit elements from Fig. 1 as implemented in WIPL-D Microwave.

Average Measured S Parameters vs. S Parameters Calculated using Model

For a particular transistor selected for illustration of model implementation in WIPL-D Microwave, equivalent circuit model elements are listed for four Vds values, 1.5, 2.0, 3.0 and 4.0 V, with Ids spanning values of 5, 10, 15 and 20 mA. Average measured S parameters are provided for drain current Ids=20 mA at the same values of drain to source voltages. This allows for direct comparison between the two means of S parameter calculations.

The comparison of S11 and S22 is presented in Fig. 3 using Smith chart format for simultaneous comparison of magnitude and phase. The S parameters calculated using model from Fig. 1 (blue traces) are in excellent agreement with average measured data (red traces). S21 and S12 are not presented in the figure due to the very high and very low magnitude values respectively which is not effectively visualized in the Smith chart format. The minor discrepancy between a model and an average device performance comes from the limitations of the relatively simple model from Fig. 1 to take into account all the features affecting the transistor performance. However, the discrepancy can be neglected for practical designs. This can be easily justified as the spread in the characteristics from one device to another, also provided by a manufacturer, is larger. For an example, the spread in transistor gain at 12 GHz is larger than 1 dB.

The results presented in Fig. 3 illustrate the importance of accurate modeling of the transistor as noticeable variations of S parameters occur for different bias points. Changes of Cgs and Rs as Vds varies do not affect significantly values of S11, while variations of S22 due to the changes in values of Rds are more obvious.

As the S parameters calculated using the transistor model match up well with the S parameters obtained by measurements, the model can be used to explore transistor performance for the case where a list of measured S parameters is not available, e.g. to quantify the influence of Ids to S21. For The intrinsic model parameters for four Ids values corresponding to the drain-source voltage Vds=2V are presented in Fig. 4. The results of S21 simulations in WIPL-D Microwave are presented in Fig. 5. As expected, the S21 values increase as Ids increases. The dominant effect leading to an increase is the change in Gm, as can be clearly seen from values highlighted in Fig. 4.

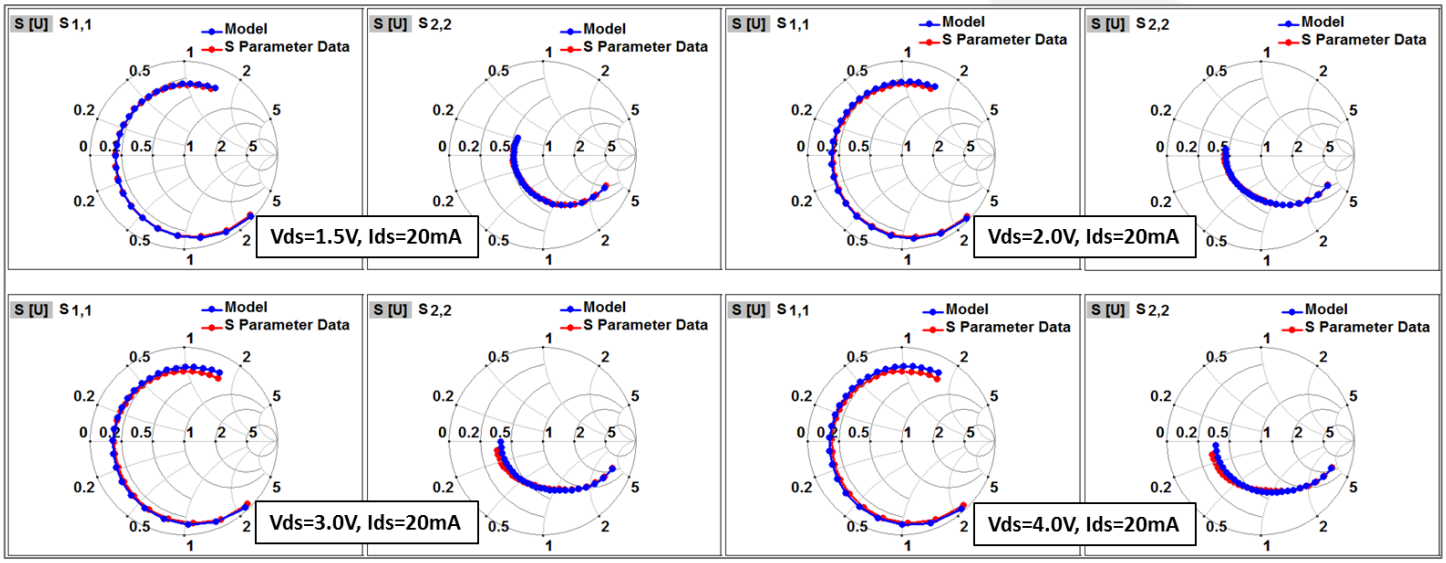

Figure 3. Comparison of S11 and S22 obtained by measurements and transistor model presented in Fig. 1 for four Vds values.

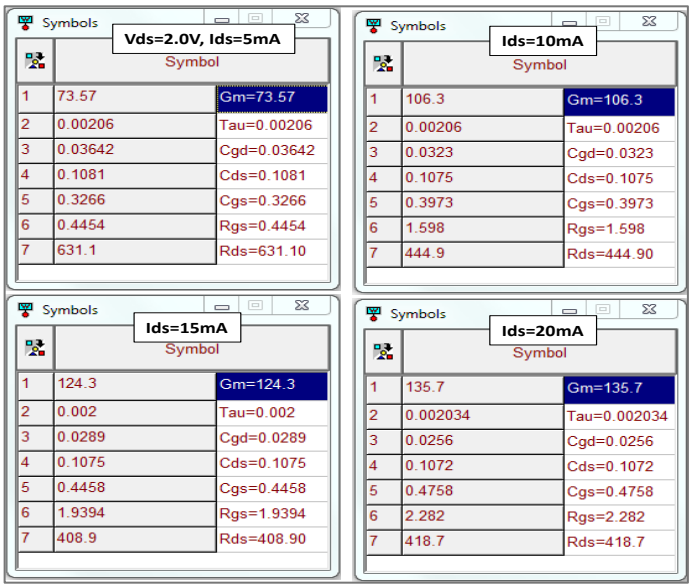

Figure 4. Four sets of values for intrinsic transistor model elements used to study the variation of S21 with Ids for Vds=2V.

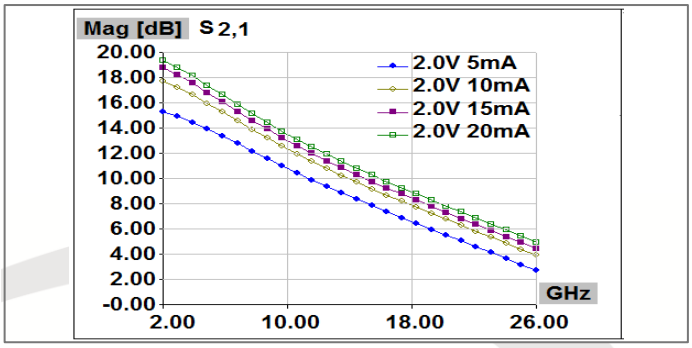

Figure 5. Variations of S21 with Ids for Vds=2V.

Conclusion

The accurate transistor characterization is a starting point to carry out an amplifier design. Lumped circuit equivalent transistor models are compact and versatile means of providing reliable S parameter data. WIPL-D Microwave provides a complete environment to implement these models.

The modeling of a commercially available low power packaged GaAs HEMT has been illustrated. The partitioning of the transistor equivalent circuit to intrinsic and extrinsic elements has been presented and physical grounds behind each of the elements explained in brief. It has been shown that S parameters calculated using the model are highly accurate and can be utilized to overcome the limitation imposed with sparsely tabulated transistor data, e.g. to find the optimal biasing point for a desired application.

For some other transistor technology, perhaps an equivalent circuit topology different from the one presented in Fig. 1 will be adequate for modeling. WIPL-D Microwave design environment provides required flexibility to implement a schematic of any commonly used linear transistor model.

Unpackaged (bare die) devices are usually utilized along with an interconnection technology that is not known by a transistor manufacturer, and equivalent circuits provided usually contain only intrinsic elements. In that case, for an accurate design, a user should use electromagnetic (EM) simulations to model accurately model the influence of an interconnecting technology to transistor performance. More details how to perform EM simulations for the specific case of bond wire connections can be found in the application note “Bond Wires as an Interconnect Technology” available for download from WIPL-D web site.